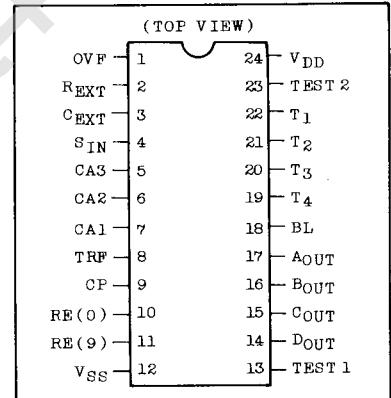## TC5001P 4-DIGIT DECADE COUNTER

TC5001P is four digit decimal counter containing latches and multiplexer circuits and equipped with the terminals of digit signal outputs for dynamic display, blanking input (for zero suppress operation) and transfer input (latch operation).
The maximum count of this counter is 9999 and three CARRY terminals are provided for carry operations required in some applications.
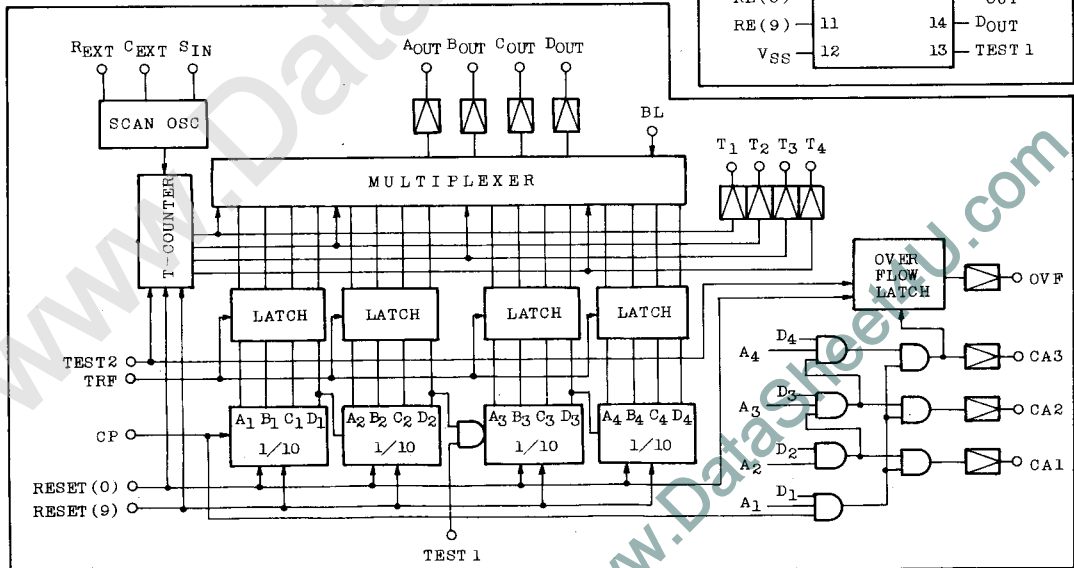Refer to TRUTH TABLE, TIMING CHART and OPERATING CONSIDERATION for the operations.

DIP 24 (6D24A-P)
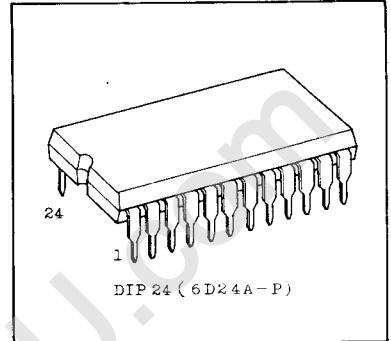
## ABSOLUTE MAXIMUM RATINGS

| CHARACTERISTIC | SYMBOL | RATING | UNIT |
|---|---|---|---|
| DC Supply Voltage | $V_{DD}$ | $V_{SS}-0.5 \sim V_{SS}+10$ | V |
| Input Voltage | $V_{IN}$ | $V_{SS}-0.5 \sim V_{DD}+0.5$ | V |
| Output Voltage | $V_{OUT}$ | $V_{SS}-0.5 \sim V_{DD}+0.5$ | V |
| DC Input Current | $I_{IN}$ | $\pm 10$ | mA |
| Power Dissipation | $P_D$ | 300 | mW |
| Storage Temperature Range | $T_{stg}$ | $-55 \sim 125$ | °C |
| Lead Temp./Time | $T_{sol}$ | 260°C · 10sec | |

## PIN ASSIGNMENT

(TOP VIEW)

| | | | |
|---|---|---|---|
| OVF | 1 | 24 | $V_{DD}$ |
| $R_{EXT}$ | 2 | 23 | TEST 2 |
| $C_{EXT}$ | 3 | 22 | $T_1$ |
| $S_{IN}$ | 4 | 21 | $T_2$ |
| CA3 | 5 | 20 | $T_3$ |
| CA2 | 6 | 19 | $T_4$ |
| CA1 | 7 | 18 | BL |
| TRF | 8 | 17 | $A_{OUT}$ |
| CP | 9 | 16 | $B_{OUT}$ |
| RE(0) | 10 | 15 | $C_{OUT}$ |
| RE(9) | 11 | 14 | $D_{OUT}$ |
| $V_{SS}$ | 12 | 13 | TEST 1 |

## BLOCK DIAGRAM

# TC5001P

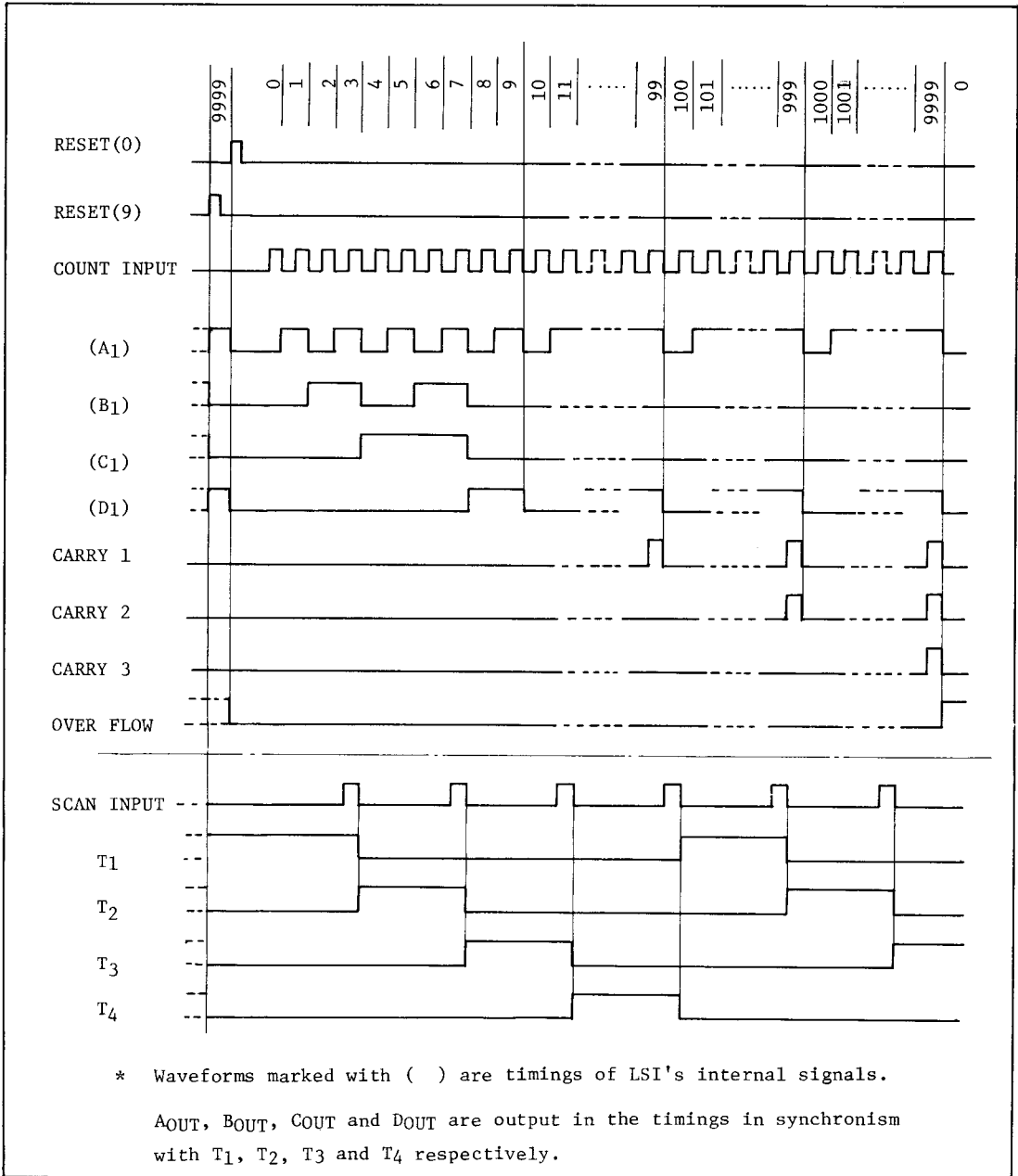DESCRIPTION OF PIN FUNCTION

| PIN No. | SYMBOL | NAME | FUNCTION |
|---|---|---|---|
| 1 | OVF | OVER FLOW | Terminal to detect OVER FLOW condition of the counter which generates "H" level when COUNT is incremented from "9999". Once set to "H", only RESET (0) can clear it to "L". |
| 2 | $R_{EXT}$ | RESISTER EXTERNAL | This is opened when external CLOCK is supplied from $S_{IN}$. If external CLOCK is not available, CLOCK can be generated by externally connecting a resistor across $S_{IN}$ and $R_{EXT}$ and a capacitor across $S_{IN}$ and $C_{EXT}$. |
| 3 | $C_{EXT}$ | CAPACITANCE EXTERNAL | |
| 4 | $S_{IN}$ | SCAN INPUT | T-COUNTER CLOCK input and T-COUNTER is changed its condition at the falling edge of $S_{IN}$. |
| 5 | CA3 | CARRY-3 | CARRY output from n-th digit / COUNTER "9999" "X999" "xx99" / "H" during CP="H" in COUNT shown at the left,"L" otherwise. |
| 6 | CA2 | CARRY-2 | |
| 7 | CA1 | CARRY-1 | |
| 8 | TRF | TRANSFER | "H" Decimal COUNTER output is transferred to MULTIPLEXER as it is. "L" COUNTER output at the time of falling edge of TRF is latched. |
| 9 | CP | COUNT INPUT | Lowest order decimal COUNTER CLOCK input and COUNTER is counted by the falling edge of CP. |
| 10 | RE (0) | RESET (0) | "H" Decimal COUNTER output is reset to "0000". This takes precedence over RE (9). "L" If RE (9) = "L", normally counted. |
| 11 | RE (9) | RESET (9) | "H" If RE (0) = "L", COUNTER output is set to "9999". "L" If RE (0) = "L", normally counted. |
| 12 | $V_{SS}$ | $V_{SS}$ | ( GND ) |

DESCRIPTION OF PIN FUNCTION

| PIN No. | SYMBOL | NAME | FUNCTION | |
|---------|--------|------|----------|--|
| 13 | $TEST_1$ | $TEST_1$ | "H" | If TEST (2) = "H", normally counted. |
| | | | "L" | If TEST (2) = "H", only lower order two digits are counted. |
| 14 | $D_{OUT}$ | D-OUTPUT | Decimal COUNTER BCD outputs.When $T_1$="H", the lowest order digit (first digit) is output, when $T_2$ = "H", the second digit is output, ... and when $T_4$ = "H", the fourth digit is output. During BLANKING all the outputs become "H". | |
| 15 | $C_{OUT}$ | C-OUTPUT | | |
| 16 | $B_{OUT}$ | B-OUTPUT | | |
| 17 | $A_{OUT}$ | A-OUTPUT | | |
| 18 | BL | BLANKING | If BL = "H", only all $A_{OUT}$ through $D_{OUT}$ (BCD OUT) become "H". | |
| 19 | $T_4$ | $T_4$ | Output to indicate the digit position of output signals $A_{OUT}$ through $D_{OUT}$ (BCD OUT) and corresponds in descending order from $T_1$. | |
| 20 | $T_3$ | $T_3$ | | |
| 21 | $T_2$ | $T_2$ | | |
| 22 | $T_1$ | $T_1$ | | |
| 23 | $TEST_2$ | $TEST_2$ | "H" | Normally counted. |
| | | | "L" | Causes $T_1$ = "L", $T_2 \sim T_4$ = "H", OVF = "H". |
| 24 | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ Power Supply (3~8 volt) | |

# TC5001P

TIMING CHART



*   Waveforms marked with (  ) are timings of LSI's internal signals.

    $A_{OUT}$, $B_{OUT}$, $C_{OUT}$ and $D_{OUT}$ are output in the timings in synchronism
    with $T_1$, $T_2$, $T_3$ and $T_4$ respectively.

TRUTH TABLE

| RESET (0) | RESET (9) | TRAN-SFER | BLAN-KING | TEST$_1$ | TEST$_2$ | A$_{OUT}$ | B$_{OUT}$ | C$_{OUT}$ | D$_{OUT}$ | T$_1$ | T$_2$ | T$_3$ | T$_4$ | OVER FLOW | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| H | * | H | L | * | H | L | L | L | L | H | L | L | L | L | Note-1 |
| L | H | H | L | * | H | H | L | L | H | H | L | L | L | X | Note-1 |
| L | L | H | L | H | H | C | C | C | C | S | S | S | S | X | |
| L | L | H | L | L | H | C' | C' | C' | C' | S | S | S | S | X | |
| * | * | L | L | * | * | LA | LA | LA | LA | X | X | X | X | X | |
| * | * | * | H | * | * | H | H | H | H | X | X | X | X | X | |
| * | * | * | * | * | L | X | X | X | X | L | H | H | H | H | |

*    Don't Care

X    Not defined

C    Count operation (all digits)

C'   Count operation (only lower order two digits)

LA   Latch operation

S    Scan operation

Note 1. SCAN INPUT = "L"

o   All the inputs/outputs (except COUNT INPUT and SCAN INPUT) are activated by "H" level.

o   COUNT INPUT ⊓    SCAN INPUT ⊓
          $t_n \rightarrow t_{n+1}$               $t_n \rightarrow t_{n+1}$

o   When used, TEST$_1$ = "H" and TEST$_2$ = "H" should be satisfied.

OPERATING CONSIDERATION

1.   RESET Operation

(1)   When the level of RESET (0) terminal is set to "H", BCD output of COUNTER is set to "0". The four digit display becomes 0000.

(2)   When the level of RESET (9) terminal is set to "H", BCD output of COUNTER is set to "9". The four digit display becomes 9999.

(3)   When both of RESET (0) terminal and RESET (9) terminal are "H", RESET (0) terminal takes precedence.

2.   SCAN Operation

(1)   SCAN signal for dynamic display applied to SCAN INPUT terminal controls the multiplexer circuit and transfers four digit information in the latches to BCD outputs one digit at a time in sequence.

OPERATING CONSIDERATION

(2) Arbitrary digit can be made real time output (completely static) by making SCAN signal DC.

(3) The digit pulses in synchronism with SCAN signal for dynamic display appear at the digit output terminals ($T_1$, $T_2$, $T_3$ and $T_4$). The digit output terminals ($T_1$, $T_2$, $T_3$ and $T_4$) are used for the digit selection circuit and for arbitrary digit zero suppress.

(4) The digit pulse is activated by the falling edge of SCAN INPUT signal.

(5) SCAN signal is supplied from the internal oscillator as shown in Fig. 1 or from the external one as shown in Fig. 2.
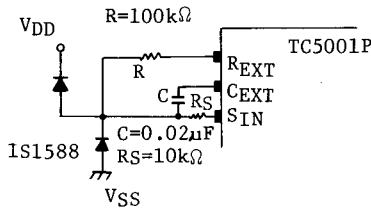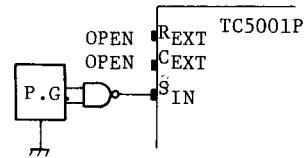


Fig. 1                    Fig. 2

$$f_{SCAN} \doteqdot \frac{1}{2.2CR} \text{ [Hz]}$$

3. Latch Operation

(1) When the level of TRANSFER terminal is "H", COUNTER information is transferred to the latches.

(2) When the level of TRANSFER terminal is charged from "H" to "L", the information transferred from COUNTER is latched.

4. Count Operation

(1) Set input terminals $TEST_1$, $TEST_2$ and TRANSFER to "H" and BLANKING terminal to "L".

(2) COUNTER is set by applying "H" level to RESET (0) or RESET (9) terminal and two RESET terminals are returned to "L".

OPERATING CONSIDERATION

(3) When the count pulse is applied to COUNT INPUT terminal, COUNTER performs its COUNT operation at the falling edge of count pulse.

(4) The maximum count is 9999 and if 9999 is exceeded, "H" level appears at OVER FLOW terminal. Removal of OVER FLOW signal can be achieved by applying"H" to RESET (0) terminal.

(5) The carry signals from 100's and 1000's digits appear at output terminals CARRY$_1$, CARRY$_2$ and CARRY$_3$.

(6) When TEST$_1$ terminal is "L", only lower order two digits of COUNTER are counted.

5. BLANKING Operation

When BLANKING terminal is set to "H", all the BCD outputs of COUNTER become "H" and this signal is used to achieve the zero suppress operation.

# TC5001P

RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0V$)

| CHARACTERISTIC | SYMBOL | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | | 3 | – | 8 | V |
| Input Voltage | $V_{IN}$ | | 0 | – | $V_{DD}$ | V |
| Operating Temp. | Topr | | –30 | – | 85 | °C |
| External Registance | $R_{EXT}$ | | 10 | 100 | 1000 | kΩ |
| External Capacitance | $C_{EXT}$ | | 10-4 | 0.02 | 1.0 | μF |

ELECTRICAL CHARACTERISTICS ($V_{SS}=0V$)

| CHARACTERISTIC | | SYMBOL | TEST CONDITIONS | $V_{DD}$ (V) | –30°C MIN. | –30°C MAX. | 25°C MIN. | 25°C TYP. | 25°C MAX. | 85°C MIN. | 85°C MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| High Level Output Voltage | | $V_{OH}$ | $|I_{OUT}| < 1\mu A$ $V_{IN}=V_{DD}, V_{SS}$ | 5 | 4.95 | – | 4.95 | – | – | 4.95 | – | V |
| Low Level Output Voltage | | $V_{OL}$ | $|I_{OUT}| < 1\mu A$ $V_{IN}=V_{DD}, V_{SS}$ | 5 | – | 0.05 | – | – | 0.05 | – | 0.05 | |
| High Level Output Current | $A_{OUT}, B_{OUT}$ $C_{OUT}, D_{OUT}$ | $I_{OH}$ | $V_{OH} = 2.5V$ $V_{IN}=V_{DD}, V_{SS}$ | 5 | –1.2 | – | –1.0 | | – | –0.75 | – | mA |
| | CARRY1,2,3 OVER FLOW $T_1,T_2,T_3,$ $T_4$ | $I_{OH}$ | | 5 | –1.2 | – | –1.0 | | – | –0.75 | – | |
| | $R_{EXT}$ $C_{EXT}$ | $I_{OH}$ | | 5 | –0.3 | – | –0.25 | | – | –0.2 | – | |
| Low Level Output Current | $A_{OUT}, B_{OUT}$ $C_{OUT}, D_{OUT}$ | $I_{OL}$ | $V_{OL} = 0.4V$ $V_{IN}=V_{DD}, V_{SS}$ | 5 | 2.4 | – | 2.0 | | – | 1.6 | – | mA |
| | CARRY1,2,3 OVER FLOW $T_1,T_2,T_3,$ $T_4$ | $I_{OL}$ | | 5 | 0.52 | – | 0.44 | | – | 0.36 | – | |
| | $R_{EXT}$ $C_{EXT}$ | $I_{OL}$ | | 5 | 0.28 | – | 0.24 | | – | 0.2 | – | |
| Input Voltage | "H" Level | $V_{IH}$ | $V_{OUT}=0.1V, 4.9V$ | 5 | 3.8 | – | 3.8 | 2.75 | – | 3.8 | – | V |
| | "L" Level | $V_{IL}$ | $|I_{OUT}| < 1\mu A$ | 5 | – | 1.2 | – | 2.25 | 1.2 | – | 1.2 | |
| Input Current | "H" Level | $I_{IH}$ | $V_{IH} = 8V$ | 8 | – | 0.2 | – | | 0.2 | – | 1.0 | μA |
| | "L" Level | $I_{IL}$ | $V_{IL} = 0V$ | 8 | – | –0.2 | – | | –0.2 | – | –1.0 | |
| Quiescent Current Consumption | | $I_{DD}$ | $V_{IN}=V_{DD}, V_{SS}$ * | 8 | – | 50 | – | – | 50 | – | 500 | μA |

* All valid input combinations

SWITCHING CHARACTERISTICS   (Ta=25°C,  $V_{SS}$=0V, $C_L$ = 50pF)

| CHARACTERISTIC | | SYMBOL | TEST CONDITIONS | $V_{DD}$(V) | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|---|
| (LOW-HIGH) Propagation Delay Time | | $t_pLH$ | COUNT INPUT — A,B,C,$D_{OUT}$ (Waveform 1) | 5 | – | 600 | 1000 | ns |
| (HIGH-LOW) Propagation Delay Time | | $t_pHL$ | | 5 | – | 600 | 1000 | |
| (LOW-HIGH) Propagation Delay Time | | $t_pLH$ | TRANSFER — A,B,C,$D_{OUT}$ (Waveform 2) | 5 | – | 400 | 1000 | |
| (HIGH-LOW) Propagation Delay Time | | $t_pHL$ | | 5 | – | 400 | 1000 | |
| (LOW-HIGH) Propagation Delay Time | | $t_pLH$ | COUNT INPUT — $CARRY_{1,2,3}$ — OVER FLOW (Waveform 3) | 5 | – | 400 | 1000 | |
| (HIGH-LOW) Propagation Delay Time | | $t_pHL$ | | 5 | – | 400 | 1000 | |
| Max. Clock Rise Time | | $t_{rCL},t_{fCL}$ | | 5 | 20 | – | – | µs |
| Min. Clear Pulse Width | | $t_{w(RE)}$ | RESET(0),(9) | 5 | – | | 1000 | ns |
| Min. Transfer Pulse Width | | $t_{w(TR)}$ | TRANSFER | 5 | – | | 1000 | |
| Input Capacity | 9, 10, 11, 18 PIN | $C_{IN}$ | | | – | 5 | 7.5 | pF |
| | 4, 13, 23 PIN | $C_{IN}$ | | | – | 7 | 10 | |
| | 8 PIN | $C_{IN}$ | | | – | 9 | 15 | |
| Max.Clock Frequency | | $f_{CL}$ | | 5 | 0.5 | 2.0 | – | MHz |

SWITCHING TIME TEST CIRCUIT
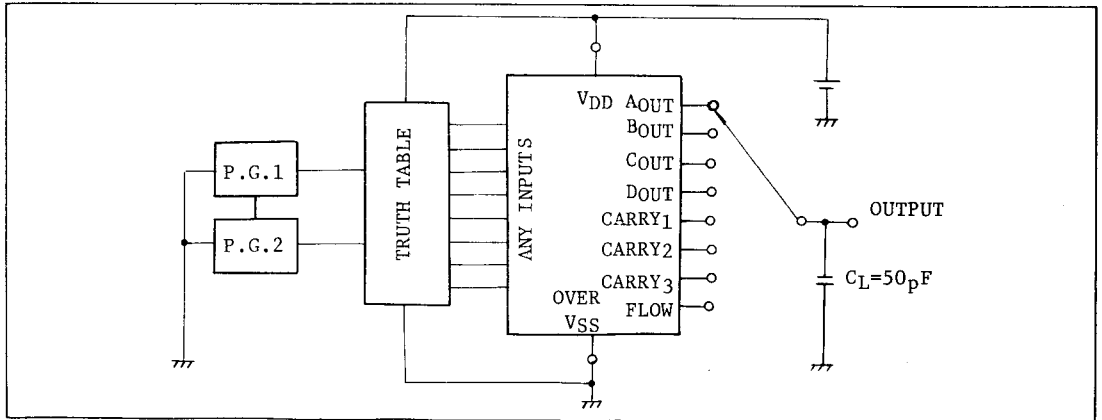
SWITCHING TIME TEST WAVEFORMS